Industry Leading High Rate/High Uniformity Blanket Silicon Etch Process for Via Reveal Applications using Rapier XE

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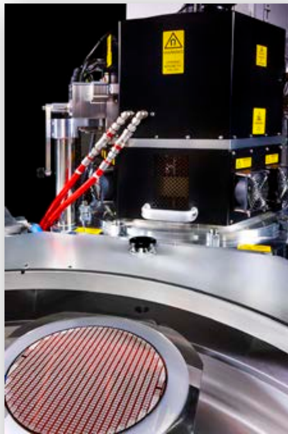
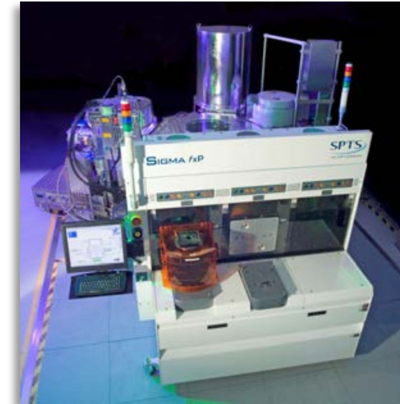
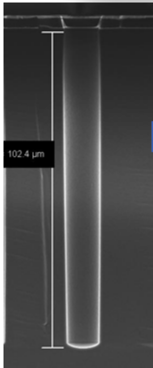
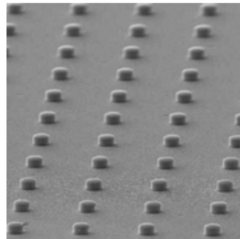
SPTS & Advanced Packaging

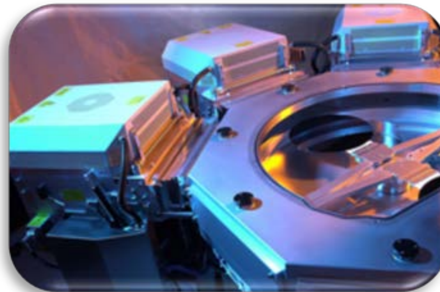


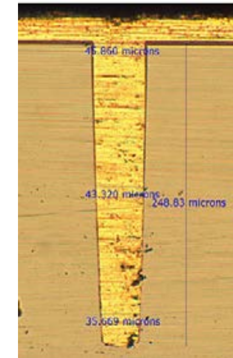
Products	Packaging Applications
Etch	TSV Via reveal Plasma dicing
CVD	Low temp TSV liners Via reveal
PVD	TSV barrier & seed UBM/RDL FO-WLP
Thermal	FO-WLP anneals Interposers Cu anneal

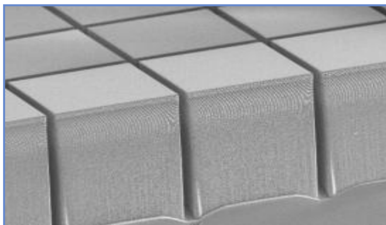


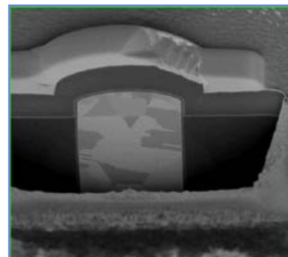


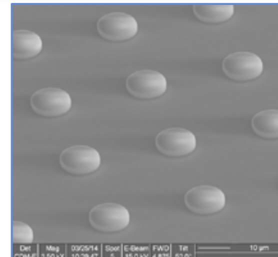












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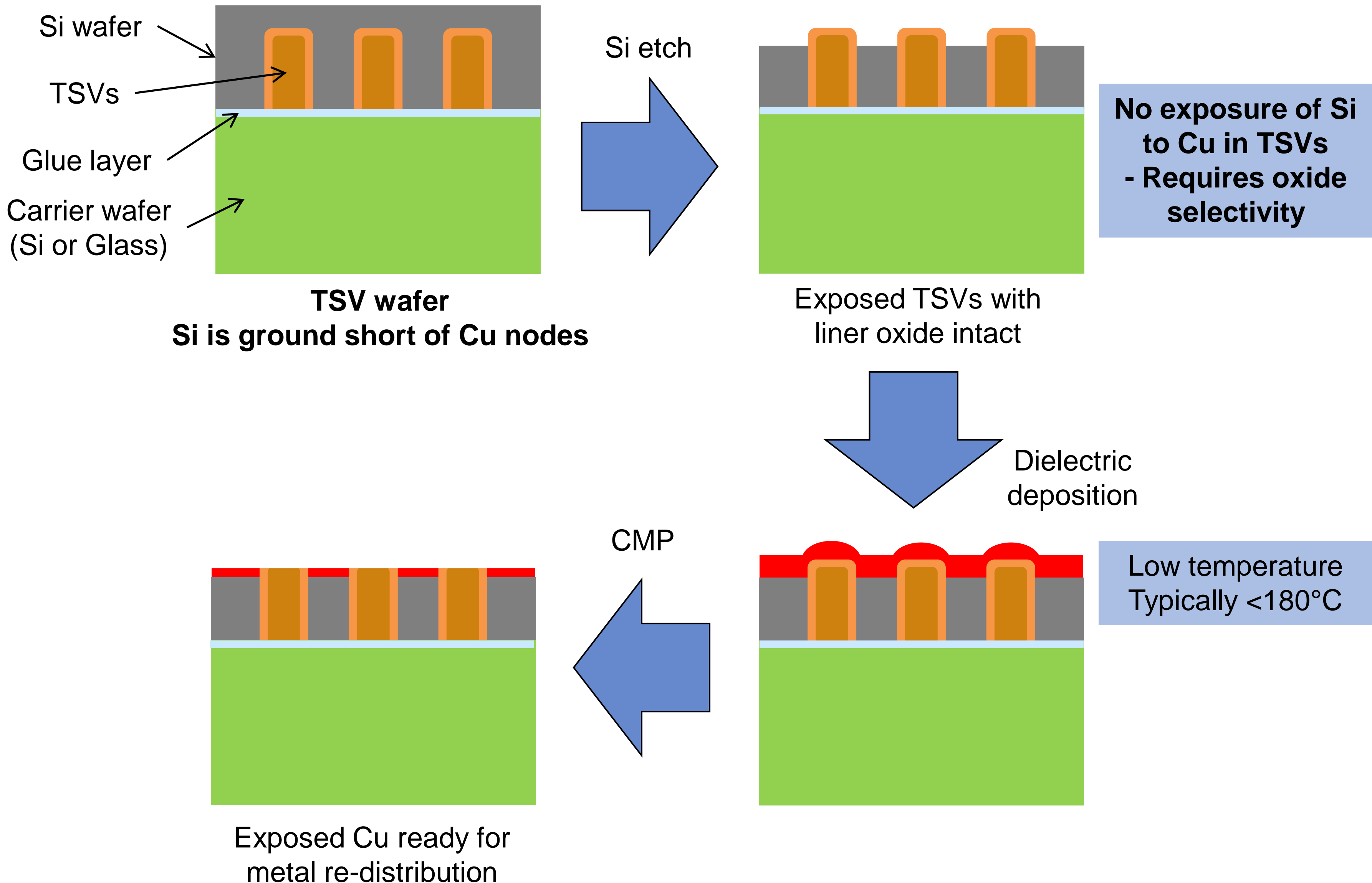
Via Reveal Process Flow



TSV wafer
Si is ground short of Cu nodes

Exposed TSVs with
liner oxide intact

Exposed Cu ready for
metal re-distribution

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SPTS Products for VR Etch

Performance

DSi

≥2.5µm/min
≤±5%

Rapier

≥4.5µm/min
≤±5%

+80%

Rapier XE

≥8.5µm/min
≤±3.5%

+89%

+240%

Highest etch rate
Best uniformity
= Lower CoO +
Higher Yield

Time

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Rapier XE Module

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- ‘Dual Source’ technology
- Recipe driven uniformity tuning
- High & uniform gas dissociation
  - Drives etch rate & uniformity
- ReVia™ *in-situ* end-point detection
  - Down to 0.01% via density
- Wafer edge protection option
  - Protect bond layer & carrier
- Same hardware for TSV etching
  - Interposer, via middle & via last
- Oxide etch capability
  - eg. Spacer etching for via last

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<1nm Si Smoothness Post Reveal

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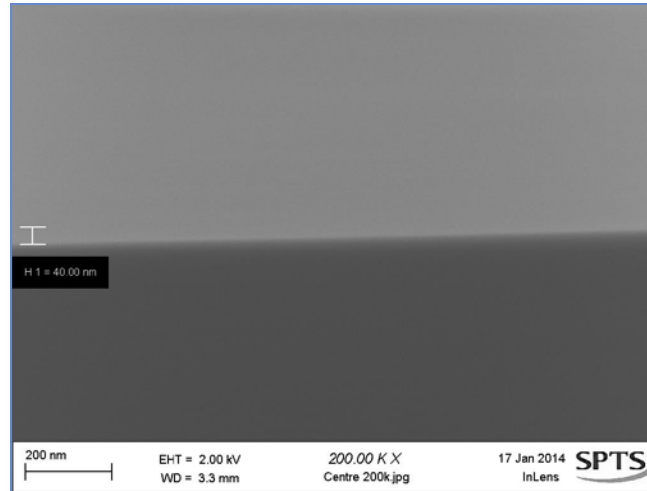
- 9µm/min, ±1.8%, 180:1 selectivity



	#1 – 15um Etch	#2 – 20um Etch	#3 – 25um Etch	#4 – Ref.
Center				
Rms / Ra / P-v (nm)	0.9 / 0.7 / 10.4	1.0 / 0.7 / 12.8	0.9 / 0.7 / 11.4	0.2 / 0.1 / 1.5

AFM customer data

Ra (average) <1nm
Rt (total, peak to valley)<13nm

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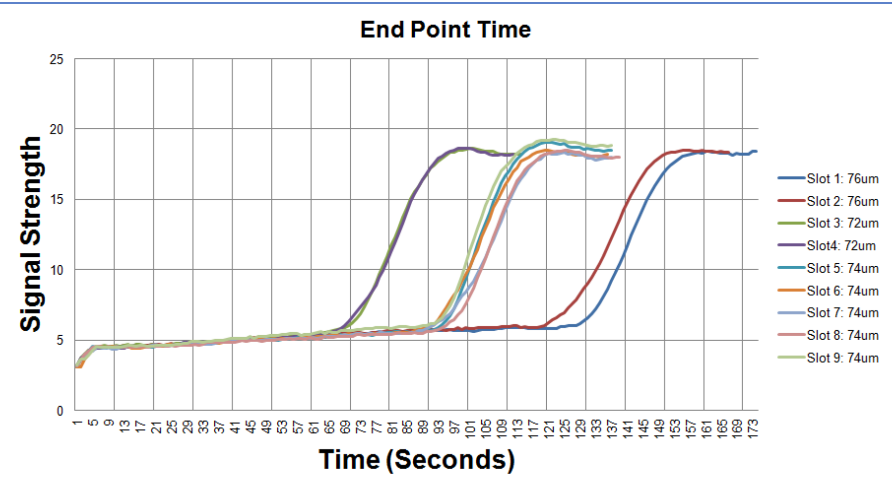
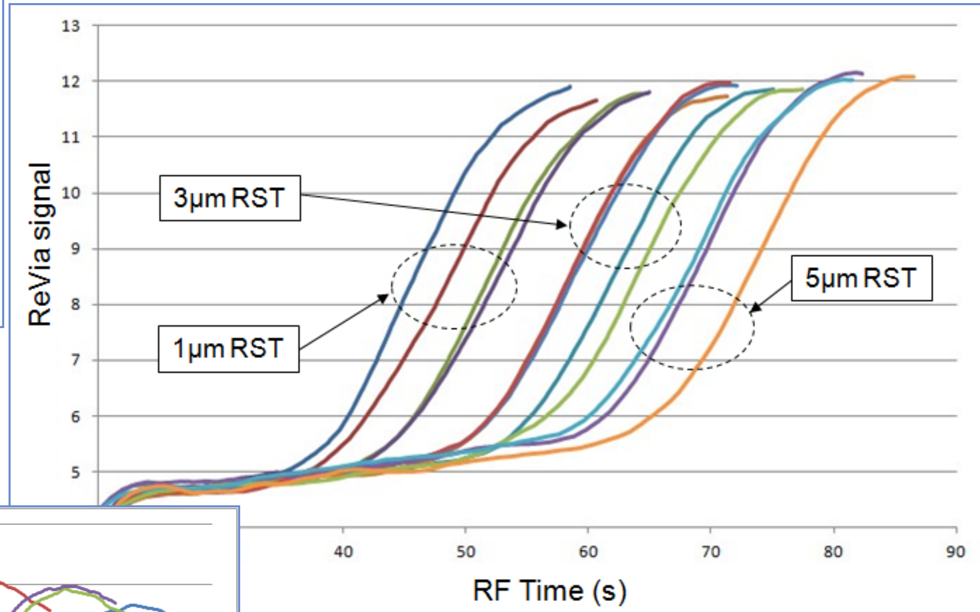
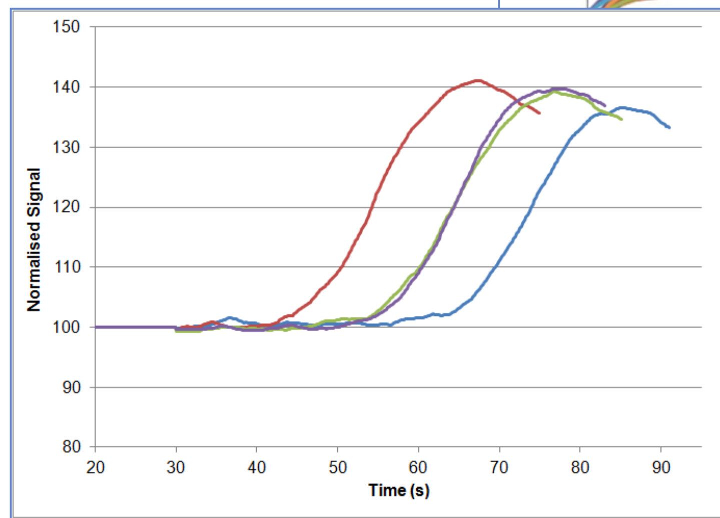
ReVia™ End-point Detection



- Built-in compensation for incoming thickness variations



- Copes with low TSV densities
  - <0.011%



Unique & robust end-pointing for any TSV layout or RST variance

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End-point Control Saves Money

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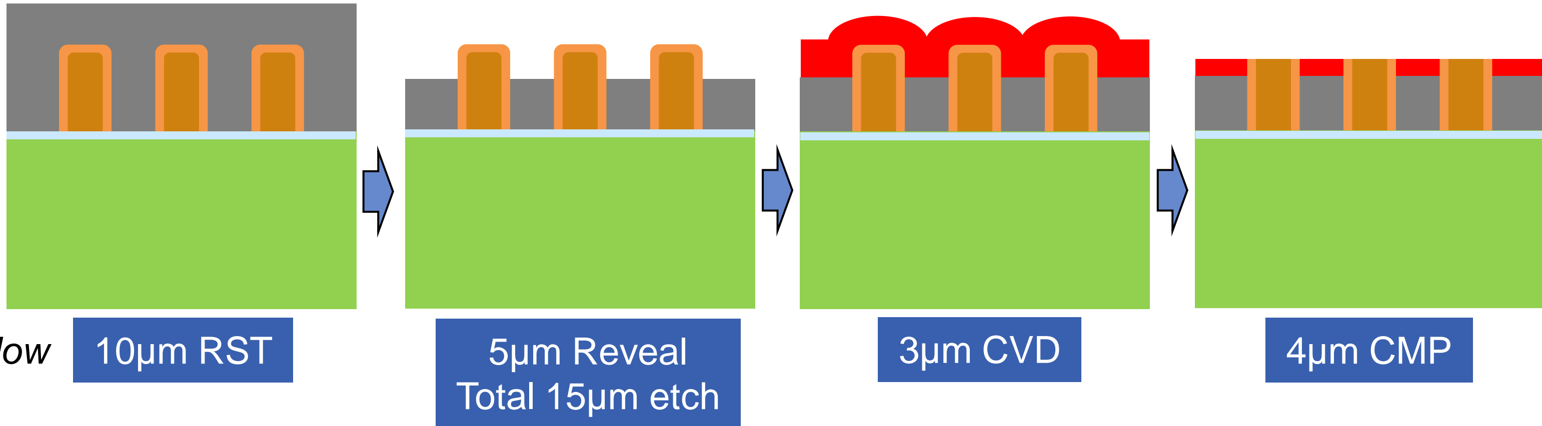
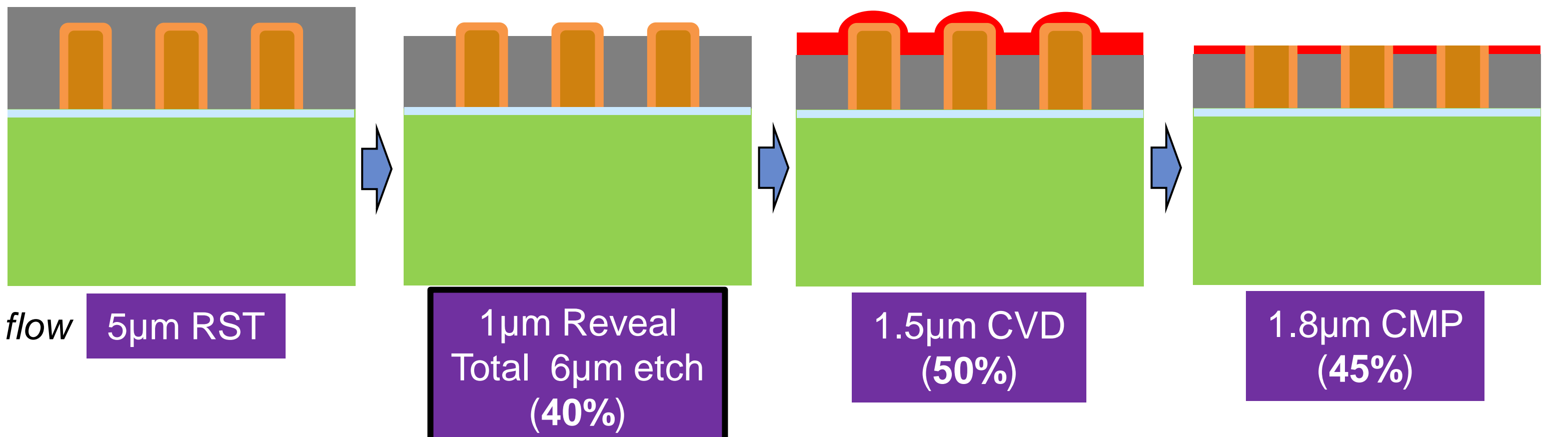
- Standard approach



- **<u>Cost Reduced</u>** approach with ReVia™



Only available with *in-situ* end-point detection (ReVia™)

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Flexibility for 3D-IC Etching

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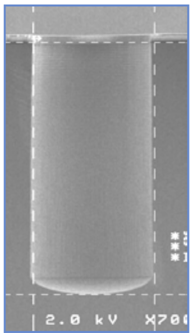
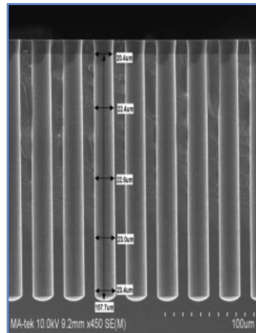
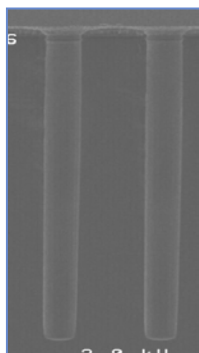
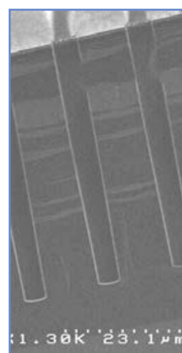
- Multiple etches from single hardware set

'Conventional' TSVs

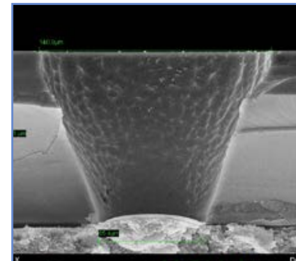
Interposer TSV

50 x 120 µm <160 nm Sc	20 x 160 µm <160 nm Sc

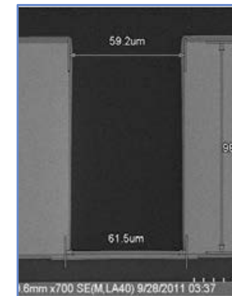
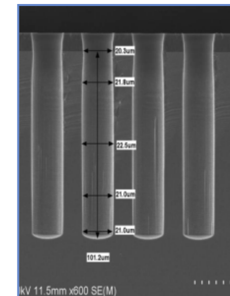



Via Middle TSV

10 x 100 µm <70 nm Sc	5 x 50 µm <6 nm Sc



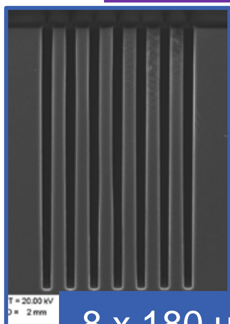
Via Last TSV
Tapered
100 µm diam
No scallops

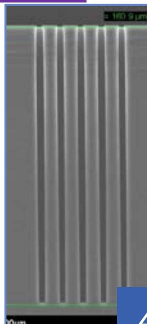
Via Last TSV
Vertical

50 x 100 µm <150 nm Sc	20 x 100 µm <150 nm Sc

***MEMS TSVs* (Poly or W fill)**

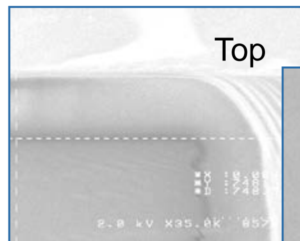


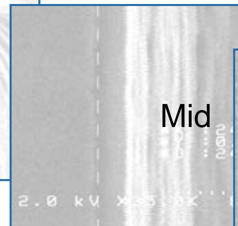
8 x 180 µm
<200nm Sc

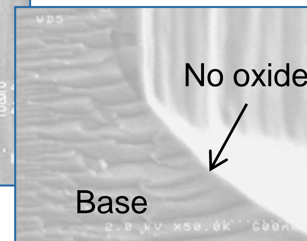


4 x 160 µm
<50 nm Sc

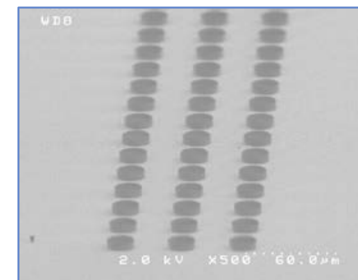
Via Last 'Spacer Etch'







Via Reveal



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Summary

- SPTS has highest performance, cost effective, etch solutions for Advanced Packaging
- Rapier XE delivers industry's highest etch rate & best uniformity
  - ≥8.5μm/min, ≤±3.5% uniformity
  - Lowest CoO, highest yield
- 'Dual source' approach allows recipe tuning of uniformity
  - Accounts for incoming residual Si thickness variations
- Smooth Si surfaces are available even at highest rate
  - Ra <1nm
- ReVia™ is the industry's only end-point detection for VR etching
  - Ensures wafer to wafer repeatability
  - Allows further cost take out due to 1μm tip height capability
  - Capability demonstrated through collaboration with IMEC
- Rapier technology also available for TSV & some oxide etch applications

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