ReVia™ Endpoint Solution for Via Reveal

Introduction

ReVia™ is a new endpoint detection (EPD) technique that can monitor the progress of "via reveal" etch processes even at remarkably low (<0.01%) via densities.

It is a unique solution that can significantly increase yields for the growing number of device manufacturers involved in emerging 3D packaging applications utilizing through-silicon vias (TSVs).

Via reveal substrates typically have a low via density and conventional EPD techniques are not successful in detecting the revealed via tips.

Benefits Summary

In-situ endpointing

- No need to pre-measure every wafer or remove wafer from system to measure progress of silicon etch

Endpoint visible with low via density

- Via density down to 0.01% measureable

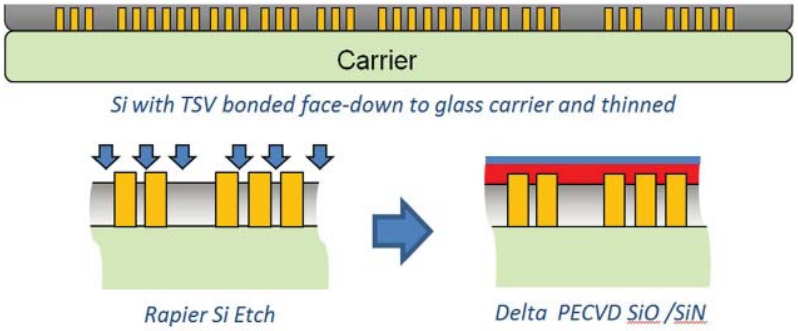
Production-worthy solution

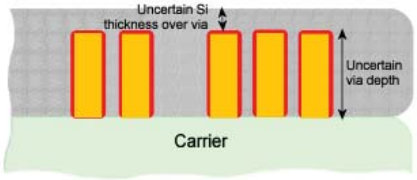
- Without in-situ endpoint "soft reveal" is not a viable production process

Reduce scrap or re-working

- Avoids over-etching or under-etching

Via Reveal Processing





Etch requirements can vary due to via depth and grind non-uniformities

Via reveal, or post-TSV processing occurs after the through silicon vias (TSVs) are formed. The wafer is then temporarily bonded, face down, onto a carrier and ground typically to within 5-10 µm of the buried TSVs. The ground Si surface is then dry etched, selectively to the TSV liner oxide, revealing the copper filled vias to a height of around 5µm.

After silicon etching, these via tips are passivated with further dielectric and then polished by chemical mechanical planarization (CMP) to expose the copper ready for RDL metallization.

Due to Total Thickness Variation (TTV) of incoming ground wafers, it is essential that the point at which the vias are revealed can be detected in-situ.

Without endpoint, the user has to independently measure the silicon thickness above the TSVs on every wafer and adjust the etch time accordingly; adding cost, complexity and risk of yield loss in the process flow.

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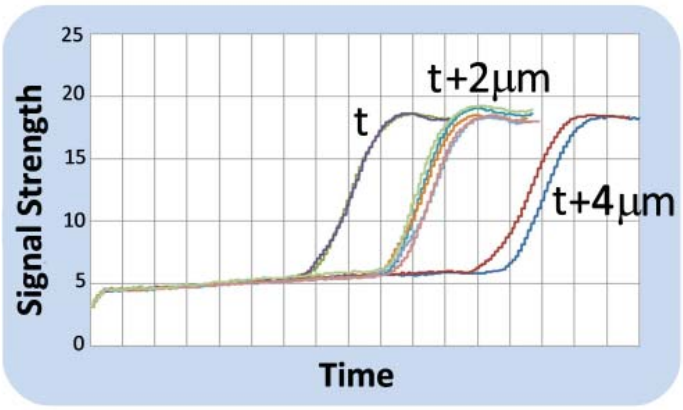
The ReVia™ solution

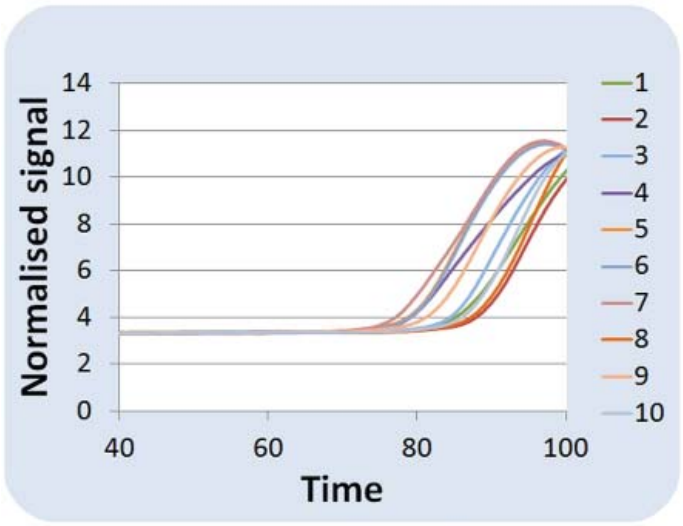
ReVia™ is a new technique which combines innovative software and hardware developments to monitor the point at which the silicon etch process begins to reveal the base of the via.

It is an extremely sensitive method which can end-point processes with very low (<0.01%) via area densities.

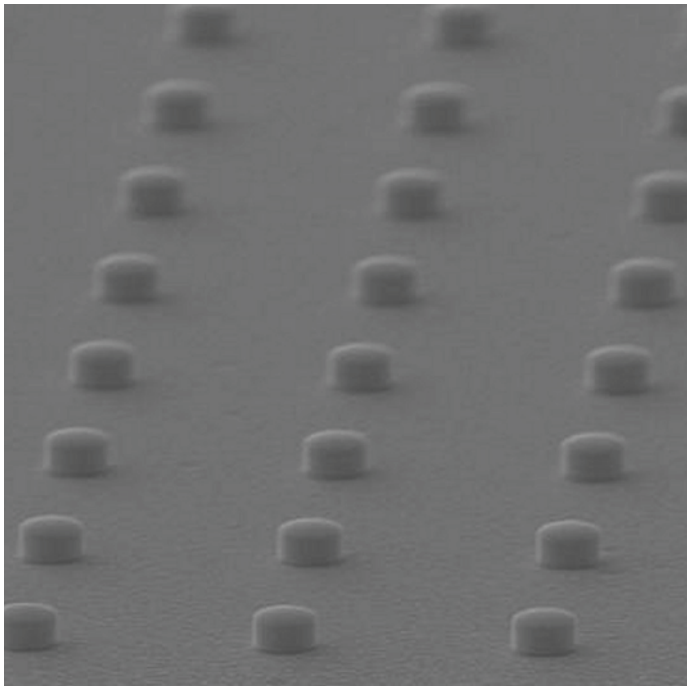
The graph below shows typical endpoint data from a batch of 9 wafers which had been intentionally ground to different thicknesses prior to silicon etching. Endpoints for the different thickness groups can clearly be seen.



Example of ReVia endpoint data from 9 wafers with 3 different post grind thicknesses (t)



Example of ReVia endpoint data from 10 wafers with an unintended range of incoming TTV



SEM image of revealed vias

Summary

Available only on SPTS' Rapier DRIE system, the ReVia™ end-point system detects the point at which the TSV tips are revealed, enabling a consistent reveal height from one wafer to the next.

This increases yields, avoids scrap and saves the device manufacturer both time and money at a point in the fabrication process where the wafers have an extremely high value.

ReVia™ can be retrofitted to existing SPTS Rapier DRIE systems.